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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/392,865	09/09/99	KITAMURA S	005702-20035

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 07/05/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/392,865	Applicant(s) Kitamura et al.
	Examiner Thien Tran	Group Art Unit 2811

☐ Responsive to communication(s) filed on _____

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 5-7, 16, and 17 is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 5-7, 16, and 17 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 17 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recitation of "memory regions extending in one direction and element separating regions extending in said direction are alternately formed" can be interpreted as setting forth structure not supported by the specification. The specification does not provide a description of memory regions extending in one direction and element separating regions extending in said direction being alternately formed.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear and confusing to determine the scope of the claim because applicant does not define the direction in the disclosure and explain how the memory regions extend in that direction.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 16-17 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al. (US 5,068,697) in view of Santin et al. (US 5,907,171).

Noda et al. discloses a nonvolatile semiconductor memory device (Fig. 4) comprising a semiconductor substrate 21; memory transistors formed on said semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data, each of said memory transistors being an electrically rewritable memory transistor including a floating gate FG formed over said semiconductor substrate via a first gate insulating film 23 and a control gate CG formed over said floating gate via a second gate insulating film 24; an oxide film (23, 25) formed on said substrate and at least on both sides of each said floating gate and both sides of each said control

gate; side walls 26 each for protecting sides of said floating gate and said control gate of each said transistor, each said side wall formed of PSG; a second silicon nitride film 29 covering surfaces of said control gate, a source diffusion layer 27, a drain diffusion layer 28 and each of said side walls of each of said memory transistors; and a wiring layer 32 formed over said second silicon nitride via an interlayer insulating film 30. Noda et al. does not disclose side walls 26 formed of silicon nitride. Phosphorus silicate glass (PSG) and silicon nitride are dielectric materials known in the art and routinely used to form protective side wall spacers in semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select either one of these materials as a suitable dielectric material for the protective side walls of Noda et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design choice. In re Leshin, 125 USPQ 416.

Regarding claim 5, the modified Noda et al. does not explicitly disclose metal silicide films formed on the surfaces of said control gate, said source/drain diffusion layers of each of said transistors. It is conventional to form metal silicide films on a control gate surface and on surfaces of source/drain regions to reduce contact resistance. Therefore, the incorporation of the conventional features into the modified Noda et al. would have been prima facie obvious.

Regarding claim 6, as a result of the incorporation of said metal silicide films on the surfaces of said source/drain diffusion layers (27, 28), the modified Noda et al. discloses said drain diffusion layer connected to a bit line 32 via said metal silicide film and said source diffusion layer

connected to a source line 31 via the metal silicide film respectively. The modified Noda et al. does not disclose the source line 31 is a common source line. However, it is old and well known in the art to form a common source line connecting source diffusion layers of adjacent memory transistors together. Therefore, forming the source line 31 as a common source line for the adjacent memory transistors would have been prima facie obvious.

Regarding claim 7, the modified Noda et al. does not explicitly disclose at least one of a low-voltage MOS transistor and a high-voltage MOS transistor formed as a peripheral circuit. It is conventional to form low-voltage transistor and high-voltage transistor as a peripheral circuit of a memory array, as shown for example by Santin et al. Therefore, the incorporation of the conventional features into the modified Noda et al. would have been prima facie obvious.

The claim limitation "formed by low-pressure CVD" in claim 16 is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

7. Applicant's arguments with respect to claims 16-17 and 5-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. **Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group**

2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Thien Tran* whose telephone number is **(703) 308-4108**. The Examiner is in the Office generally between the hours of 7:00AM to 5:30PM (Eastern Standard Time) Monday through Thursday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **(703) 308-0956**.

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July 2, 2000

Steven Loke